IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Peter D. BREWER	Examiner:	Thanhha S. Pham
Serial No.:	10/787,276	Art Unit:	2813
Filed:	February 25, 2004	Our Ref:	B-4712 620052-7
For:	"SELF-MASKING DEFECT REMOVING METHOD"	Date:	May 3, 2007

SUPPLEMENTAL DECLARATION OF PETER D. BREWER

PURSUANT TO 37 C.F.R. § 1.131 OR, IN THE ALTERNATIVE, 37 C.F.R. § 1.132

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450a

I, Peter D. Brewer, declare and say:

1. I am the inventor named in the above-identified application.

2. I refer to and incorporate by reference my earlier declaration pursuant to 37 C.F.R. 1.131 executed on September 5, 2006 and filed in the above-identified application. That earlier declaration stated that I had completed the invention disclosed and claimed in the above-identified application in the United States of America no later than November 8, 2001. This supplemental declaration further explains the invention that was completed no later than November 8, 2001. In addition, this supplemental

declaration updates the declaration executed on September 5, 2006 in reference to the amendment to claim 1 presented in the response filed with this supplemental declaration.

3. As noted in the declaration executed on September 5, 2006, Exhibit A to that declaration was a copy of a "Progress, Status and Management Report" for research on "Antimonide Based Compound Semiconductors (ABCS)" that I helped to prepare. The date of the report was stated on its cover: November 8, 2001. Irrelevant material was been redacted from the copy of the report attached as Exhibit A. The report evidenced actual reduction to practice of the invention claimed in this application before November 8, 2001.

4. The "Description of Progress" on page two of the "Progress, Status and Management Report" attached as Exhibit A to the declaration executed on September 5, 2006 contained a section that I wrote. It described research directed to a "substrate transfer technology focused on the preparation of the MBE grown epi-layer surfaces prior to wafer bonding and processes for selectively removing GaSb substrates after wafer bonding." "Morphological growth-defects on the surface of the Sb-based epilayers" are identified as problems because these defects "interfere with the bonding of the GaSb epilayers and the sapphire substrates." The solution was "a self-masking process for removing growth defects form the surface of the MBE grown Sb-based epilayers."

5. As stated in the "Progress, Status and Management Report" attached as Exhibit A to the declaration executed on September 5, 2006, the "self-masking process"

involves four processing steps: "1) coating the surface of the wafer with a thick photoresist layer (5-10 microns), 2) dry-etching the resist layer to a thickness of ~0.5 microns (to reveal the tops of the defect structures but protecting the remainder of the semiconductor surface), 3) wet chemical etching of the exposed defect structures, and 4) stripping of the remaining photoresist layer."

6. The "Progress, Status and Management Report" attached as Exhibit A observed that "this process effectively removes the protruding defect structures from the surface of the semiconductor wafer without [affecting] the surrounding epilayer material." The "Report" noted the successful results of the process: "[i]nitial results using this process to prepare as-grown HBT wafers for bonding to sapphire substrates indicate enhanced bonding yields as a result of eliminating the morphological growth defects. In these experiments, bonding surface area yields as high as 94% were obtained."

7. The step of "1) coating the surface of the wafer with a thick photoresist layer (5-10 microns)" will inherently result in the formation of a layer of photoresist on the surface of the wafer that will have a planar surface on its top surface, that is, the surface not in contact with the wafer. The reason for this is the thick photoresist will be planarized by its own surface tension and viscosity. The defects will not affect the planarity of the surface of the photoresist layer because the layer is much thicker than the defects. Note that the second step is "2) dry-etching the resist layer to a thickness of ~0.5 microns (to reveal the tops of the defect structures but protecting the remainder of the semiconductor surface)," which indicates that the defect structures will have heights

above the general surface of the wafer of no more than about one-tenth to one twentieth of the thickness of the thick photoresist layer.

8. I attach as Exhibits B and C to this supplemental declaration copies, respectively, of two articles: Jun-Bo Yoon, et al., *Planarization and Trench Filing on Sever Surface Topography with Thick Photoresist for MEMS*, SPIE Vol. 3511 (September 1998), at pp. 297-306 ("Yoon, et al.") and Peter C. Sukanek, *A Model for Spin Coating with Topography*, 136 (No. 10) J. Electrochemical Soc. 3019-3026 (October 1989)("Sukanek").

9. Yoon, et al. (Exhibit B) shows that to achieve a value of planarity (β) greater than 95% (0.95) the value of the thickness of the photoresist (d_0) relative to the topography of the surface (t_0) the value of d_0/t_0 must be greater than about six (6) for AZ4562 photoresist. See Figure 6(b) of Yoon, et al. at p. 303. The defect structures discussed in my Exhibit A have heights of between one and ten microns. Persons of skill in the art will understand that typical defects are crystallographic defects (also known as oval defects) and will have a height of about one micron and that defects with a greater height are only occasionally observed and are easily located and removed by known processes. Six times the height of the typical defect is 6.0 microns. A "thick photoresist layer (5-10 microns)" therefore will have good planarity. The planarity will be greater than 90%.

10. Sukanek (Exhibit B) discusses some of the physical factors that result in greater planarity as a result of using thick photoresist films. Sukanek assumes (at page 3020, item h) that the characteristic height of the substrate variations α_Φ (that is, the topography of the defects on the surface) is much less than L (the thickness of the

photoresist). Sukanek states in his abstract that the "viscosity and surface tension of the film [of photoresist], together with their variation with solvent content, play an important role in determining whether planar or conformal surfaces are achieved. Surface tension tends to planarize the film, whereas surface tension gradients tend to make the film more conformal. If viscosity rises very quickly as a result of solvent evaporation, the film topography becomes 'frozen-in,' and surface forces cannot planarize." This behavior is described mathematically in equation 39 on page 3022 and is described in words in the paragraph below it: "[f]rom this result, it s seen that a planar surface (y_{ns}=0) is achieved . . . when the surface tension is very large."

11. Accordingly, a person of skill would know that the step of "1) coating the surface of the wafer with a thick photoresist layer (5-10 microns)" would inherently result in the formation of a layer of photoresist on the surface of the wafer that will have a planar surface on the top surface of the photoresist

12. I understand that claim 1 of this application is being amended to read as follows:

A method for removing defects from a semiconductor surface, comprising:

coating the semiconductor surface and the defects with a protective layer, wherein the protective layer has a planar top surface;

thinning the protective layer to selectively reveal top portions of the defects;

removing the defects; and

removing the protective layer.

This method is disclosed in Exhibit A, the "Progress, Status and Management Report." The "protective layer" reads on the "thick photoresist layer," which as mentioned above, inherently had a planar top surface because of its own surface tension and viscosity.

I declare further that all statements made herein of my own knowledge are true; that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patents issuing thereon.

Date: May 3, 2007

Peter D. Brewer